ABSTRACT OF THE DISCLOSURE

A network switch system (10) is disclosed, in which a plurality of switch fabric devices (20) are interconnected according to a ring arrangement, each of the switch fabric devices (20) including therein switch interfaces (22) coupled to corresponding network switches (14, 16). Each switch fabric device includes a plurality of ring paths (24), each of which is associated with a receive ring interface (26R) and a transmit ring interface (26X). Each ring path (24) includes a circular buffer (44) having a plurality of entries, each of which is associated with valid logic (50). The valid logic (50) for each entry presents valid signals on valid lines (WV, RV) to the receive and transmit domains of the ring path (24), and receives signals on write and read word request lines (WRW, RDW) therefrom. Control of the access to the circular buffer (44) is made according to the write and read word request lines (WRW, RDW) for the corresponding entries of the circular buffer (44) to which write pointers and read pointers point. The write word request line (WRW) sets the valid lines (WV, RV) for the corresponding entry in each of the two clock domains, while the read word request line (RDW) resets these valid lines (WV, RV) for that entry. Differences in clock frequency between the receive and transmit clock domains are thus compensated, with a minimum latency.